Last update: Jan 04, 2007

WRTLT '06 in Fukuoka, JAPAN

The Seventh Workshop on RTL and High Level Testing

November 23-24, 2006, Institute of System LSI Design Industry, Fukuoka, JAPAN

In conjunction with the 15th Asian Test Symposium (ATS'06) in Fukuoka

Sponsored by
IEEE Computer Society Test Technology Technical Council
Kyushu Institute of Technology
In cooperation with
Technical Group on Dependable Computing, IEICE

INDEX

Scope

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'06, the seventh workshop, will be held in conjunction with the 15th Asian Test Symposium (ATS '06) in Fukuoka, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices.

Areas of interest include but are not limited to:

- Functional fault modeling
- Relationship between RTL and gate level testing
- RTL ATPG
- High level approaches for testing
- RTL DFT
- SoC Testing
- RTL BIST

Submissions

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. All submissions should besent to the following address as Postscript or PDF attachment.

wrtlt06-submission@ip.elec.mie-u.ac.jp

Key Dates

Submission deadline: ~~July 28, 2006~~ Augst 4, 2006
Notification of acceptance: September 11, 2006
Camera ready due: October 9, 2006

Photocopies of accepted papers will be handed out to the attendees at the workshop site.

Workshop Location

The workshop place, the Institute of System LSI Design Industry, is located at Fukuoka city in Kyusyu Island, JAPAN. It takes 45 minutes by bus from Fukuoka International Airport, and 35 minutes by bus from JR (Japan Railways) Hakata station. Two hotels, Sea Hawk Hotel and Hotel Twins Momochi, are in walking distance (3-5 minutes on foot). Many hotels are in close distance(10-20 minutes by bus).
Symposium Location Map.

You can find more information in the download pdf file.
Download

Workshop Registration

WRTLT'06 advance registration instructions and its registration form:
Download (pdf)
Download (Word)

General Information

Japan is a bow-shaped archipelago lying to the east of the Asian Continent. The local self-governing bodies of Japan consist of prefectures and municipalities. Fukuoka Prefecture, located at the northeast part of Kyusyu Island in Japan, is divided into 24 cities, 64 towns, and 8 village. The prefecture has 4,957,000 people, which means 3.9% of the national population, making it the 9th largest in Japan. Fukuoka City and Kitakyushu City in the prefecture each have over one million people. The prefecture covers an area of approximately 4971 square kilometers, tha is 1.3 % of the national land area. The annual average temperature is 62.8F, and average precipitation is 2,083mm.

More information about Fukuoka Prefecture is shown in the following Web Site:
http://www.pref.fukuoka.lg.jp/wbase.nsf/doc/kikaku_guide_d090100.htm

Further Information

E-mail: wrtlt06@ip.elec.mie-u.ac.jp

Organizing Committee

General Chair:	Kazuhiko Iwasaki, Tokyo Metropolitan University iwasaki@eei.metro-u.ac.jp
General Vice-Chair:	Tomoo Inoue, Hiroshima City University tomoo@im.hiroshima-cu.ac.jp
Program Chair:	Michiko Inoue, Nara Institute of Science and Technology kounoe@is.naist.jp
Finance Chair:	Masaki Hashizume, University of Tokushima tume@ee.tokushima-u.ac.jp
Publicity Chair:	Tsuyoshi Shinogi, Mie University shinogi@elec.mie-u.ac.jp
Publications Chair:	Hiroshi Yokoyama, Akita University yokoyama@ie.akita-u.ac.jp
Registration Chair:	Hideyuki Ichihara, Hiroshima City University ichihara@im.hiroshima-cu.ac.jp
Local Arrangements Chair:	Xiaoqing Wen, Kyushu Institute of Technology wen@cse.kyutech.ac.jp
Audio Visual Chair:	Takeshi Asakawa, Tokai University asakawa@tokai.ac.jp
Industry Liaison:	Michinobu Nakao, Renesas Technology nakao.michinobu@renesas.com
ATS Liaison:	Yukiya Miura, Tokyo Metropolitan University miura@eei.metro-u.ac.jp
Ex Officio:	Hideo Fujiwara, Nara Institute of Science and Technology fujiwara@is.naist.ac.jp

Program Committee

Chair	Michiko Inoue (NARA Institute of Science and Technology, Japan)
Members	Tsin-Yuan Chang (National Tsing Hua University, Taiwan)
	Satoshi Fukumoto (Tokyo Metropolitan University, Japan)
	Ian G. Harris (University of California, Irvine, USA)
	Kazumi Hatayama (STARC, Japan)
	Terumine Hayashi (Mie University, Japan)
	Niraj K. Jha (Princeton University, USA)
	Ramesh Karri (Polytechnic University, USA)
	Erik Larsson (Linkopings Universitet, Sweden)
	Huawei Li (Chinese Academy of Sciences, China)
	Xiaowei Li (Chinese Academy of Sciences, China)
	Masahide Miyazaki (Renesas Technology Corp., Japan)
	Zainalabedin Navabi (Northeastern University, USA)
	Sule Ozev (Duke University, USA)
	Ilia Polian (Albert Ludwigs University of Freiburg, Germany)
	Kewal K. Saluja (University of Wisconsin, USA)
	Sying-Jyan Wang (National Chung-Hsing University, Taiwan)
	Sun Yihe (Tsinghua University, China)
	Tomokazu Yoneda (NARA Institute of Science and Technology, Japan)
	Dafang Zhang (Hunan University, China)

WRTLT Steering Committee

Chair:	Hideo Fujiwara (NAIST, Japan)
Members:	Terumine Hayashi (Mie University, Japan)
	Tomoo Inoue (Hiroshima City University, Japan)
	Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan)
	Erik Larsson (Linkoeping University, Sweden)
	Xiaowei Li (Chinese Academy of Sciences, China)
	Alex Orailoglu(University of California, San Diego, USA)
	Kewal K. Saluja (University of Wisconsin, USA)
	Hideo Tamamoto (Akita University, Japan)
	J. Paulo Teixeira (IST/INESC, Portugal)
	Dong Xiang (Tsinghua University, China)
	Dafang Zhang (Hunan University, China)

Scope

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'06, the seventh workshop, will be held in conjunction with the 15th Asian Test Symposium (ATS '06) in Fukuoka, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices.

Areas of interest include but are not limited to:

- Functional fault modeling
- Relationship between RTL and gate level testing
- RTL ATPG
- High level approaches for testing
- RTL DFT
- SoC Testing
- RTL BIST

Submissions

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. All submissions should besent to the following address as Postscript or PDF attachment.

wrtlt06-submission@ip.elec.mie-u.ac.jp

Key Dates

Submission deadline: ~~July 28, 2006~~ Augst 4, 2006
Notification of acceptance: September 11, 2006
Camera ready due: October 9, 2006

Photocopies of accepted papers will be handed out to the attendees at the workshop site.

Workshop Location

The workshop place, the Institute of System LSI Design Industry, is located at Fukuoka city in Kyusyu Island, JAPAN. It takes 45 minutes by bus from Fukuoka International Airport, and 35 minutes by bus from JR (Japan Railways) Hakata station. Two hotels, Sea Hawk Hotel and Hotel Twins Momochi, are in walking distance (3-5 minutes on foot). Many hotels are in close distance(10-20 minutes by bus).
Symposium Location Map.

You can find more information in the download pdf file.
Download

Workshop Registration

WRTLT'06 advance registration instructions and its registration form:
Download (pdf)
Download (Word)

General Information

Japan is a bow-shaped archipelago lying to the east of the Asian Continent. The local self-governing bodies of Japan consist of prefectures and municipalities. Fukuoka Prefecture, located at the northeast part of Kyusyu Island in Japan, is divided into 24 cities, 64 towns, and 8 village. The prefecture has 4,957,000 people, which means 3.9% of the national population, making it the 9th largest in Japan. Fukuoka City and Kitakyushu City in the prefecture each have over one million people. The prefecture covers an area of approximately 4971 square kilometers, tha is 1.3 % of the national land area. The annual average temperature is 62.8F, and average precipitation is 2,083mm.

More information about Fukuoka Prefecture is shown in the following Web Site:
http://www.pref.fukuoka.lg.jp/wbase.nsf/doc/kikaku_guide_d090100.htm

Further Information

E-mail: wrtlt06@ip.elec.mie-u.ac.jp

Organizing Committee

General Chair:	Kazuhiko Iwasaki, Tokyo Metropolitan University iwasaki@eei.metro-u.ac.jp
General Vice-Chair:	Tomoo Inoue, Hiroshima City University tomoo@im.hiroshima-cu.ac.jp
Program Chair:	Michiko Inoue, Nara Institute of Science and Technology kounoe@is.naist.jp
Finance Chair:	Masaki Hashizume, University of Tokushima tume@ee.tokushima-u.ac.jp
Publicity Chair:	Tsuyoshi Shinogi, Mie University shinogi@elec.mie-u.ac.jp
Publications Chair:	Hiroshi Yokoyama, Akita University yokoyama@ie.akita-u.ac.jp
Registration Chair:	Hideyuki Ichihara, Hiroshima City University ichihara@im.hiroshima-cu.ac.jp
Local Arrangements Chair:	Xiaoqing Wen, Kyushu Institute of Technology wen@cse.kyutech.ac.jp
Audio Visual Chair:	Takeshi Asakawa, Tokai University asakawa@tokai.ac.jp
Industry Liaison:	Michinobu Nakao, Renesas Technology nakao.michinobu@renesas.com

ATS Liaison:	Yukiya Miura, Tokyo Metropolitan University miura@eei.metro-u.ac.jp
Ex Officio:	Hideo Fujiwara, Nara Institute of Science and Technology fujiwara@is.naist.ac.jp

Program Committee

Chair	Michiko Inoue (NARA Institute of Science and Technology, Japan)
Members	Tsin-Yuan Chang (National Tsing Hua University, Taiwan)
	Satoshi Fukumoto (Tokyo Metropolitan University, Japan)
	Ian G. Harris (University of California, Irvine, USA)
	Kazumi Hatayama (STARC, Japan)
	Terumine Hayashi (Mie University, Japan)
	Niraj K. Jha (Princeton University, USA)
	Ramesh Karri (Polytechnic University, USA)
	Erik Larsson (Linkopings Universitet, Sweden)
	Huawei Li (Chinese Academy of Sciences, China)
	Xiaowei Li (Chinese Academy of Sciences, China)
	Masahide Miyazaki (Renesas Technology Corp., Japan)
	Zainalabedin Navabi (Northeastern University, USA)
	Sule Ozev (Duke University, USA)
	Ilia Polian (Albert Ludwigs University of Freiburg, Germany)
	Kewal K. Saluja (University of Wisconsin, USA)
	Sying-Jyan Wang (National Chung-Hsing University, Taiwan)
	Sun Yihe (Tsinghua University, China)
	Tomokazu Yoneda (NARA Institute of Science and Technology, Japan)
	Dafang Zhang (Hunan University, China)

WRTLT Steering Committee

Chair:	Hideo Fujiwara (NAIST, Japan)
Members:	Terumine Hayashi (Mie University, Japan)
	Tomoo Inoue (Hiroshima City University, Japan)
	Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan)
	Erik Larsson (Linkoeping University, Sweden)
	Xiaowei Li (Chinese Academy of Sciences, China)
	Alex Orailoglu(University of California, San Diego, USA)
	Kewal K. Saluja (University of Wisconsin, USA)
	Hideo Tamamoto (Akita University, Japan)
	J. Paulo Teixeira (IST/INESC, Portugal)
	Dong Xiang (Tsinghua University, China)
	Dafang Zhang (Hunan University, China)

General Chair
Kazuhiko Iwasaki
Tokyo Metropolitan University
iwasaki@eei.metro-u.ac.jp

General Vice-Chair
Tomoo Inoue
Hiroshima City University
tomoo@im.hiroshima-cu.ac.jp

Program Chair
Michiko Inoue
Nara Institute of Science and Technology
kounoe@is.naist.jp

Finance Chair
Masaki Hashizume
University of Tokushima
tume@ee.tokushima-u.ac.jp

Publicity Chair
Tsuyoshi Shinogi
Mie University
shinogi@elec.mie-u.ac.jp

Publications Chair
Hiroshi Yokoyama
Akita University
yokoyama@ie.akita-u.ac.jp

Registration Chair
Hideyuki Ichihara
Hiroshima City University
ichihara@im.hiroshima-cu.ac.jp

Local Arrangements Chair
Xiaoqing Wen
Kyushu Institute of Technology
wen@cse.kyutech.ac.jp

Audio Visual Chair
Takeshi Asakawa
Tokai University
asakawa@tokai.ac.jp

Industry Liaison
Michinobu Nakao
Renesas Technology
nakao.michinobu@renesas.com

ATS Liaison
Yukiya Miura
Tokyo Metropolitan University
miura@eei.metro-u.ac.jp

Ex Officio
Hideo Fujiwara
Nara Institute of Science and Technology
fujiwara@is.naist.ac.jp

CALL FOR PAPERS

WRTLT'06

The Seventh Workshop on RTL and High Level Testing

November 23-24, 2006, Institute of System LSI Design Industry, Fukuoka, JAPAN

In conjunction with the 15th Asian Test Symposium (ATS'06) in Fukuoka

Sponsored by

IEEE Computer Society Test Technology Technical Council
Kyushu Institute of Technology

In cooperation with

Technical Group on Dependable Computing, IEICE

SCOPE

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. WRTLT'06, the seventh workshop, will be held in conjunction with the 15th Asian Test Symposium (ATS'06) in Fukuoka, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip(SoC) devices.
Areas of interest include but are not limited to:

- Functional fault modeling
- RTL ATPG
- RTL DFT
- RTL BIST
- Relationship between RTL and gate level testing
- High level approaches for testing
- SoC testing

SUBMISSIONS

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. All submissions should be sent to the following address as Postscript or PDF attachment.

wrtlt06-submission@ip.elec.mie-u.ac.jp

KEY DATES

Submission deadline: July 28, 2006
Notification of acceptance: September 11, 2006
Camera ready due: October 9, 2006

Photocopies of accepted papers will be handed out to the attendees at the workshop site.

FURTHER INFORMATION

WWW: http://www.ip.elec.mie-u.ac.jp/wrtlt06/
E-mail: wrtlt06@ip.elec.mie-u.ac.jp

Program Committee

Chair: Michiko Inoue, Japan
Tsin-Yuan Chang, Taiwan
Satoshi Fukumoto, Japan
Ian G. Harris, USA
Kazumi Hatayama, Japan
Terumine Hayashi, Japan
Niraj K. Jha, USA
Ramesh Karri, USA
Erik Larsson, Sweden
Huawei Li, China
Xiaowei Li, China
Masahide Miyazaki, Japan
Zainalabedin Navabi, USA
Sule Ozev, USA
Ilia Polian, Germany
Kewal K. Saluja, USA
Sying-Jyan Wang, Taiwan
Sun Yihe, China
Tomokazu Yoneda, Japan
Dafang Zhang, China

WRTLT Steering Committee

Chair: Hideo Fujiwara (NAIST, Japan)
Terumine Hayashi(Mie University, Japan)
Tomoo Inoue (Hiroshima City University, Japan)
Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan)
Erik Larsson (Linkoeping University, Sweden)
Xiaowei Li (Chinese Academy of Sciences, China)
Alex Orailoglu(University of California, San Diego, USA)
Kewal K. Saluja (University of Wisconsin, USA)
Hideo Tamamoto (Akita University, Japan)
J. Paulo Teixeira (IST/INESC, Portugal)
Dong Xiang (Tsinghua University, China)
Dafang Zhang (Hunan University, China)

(6-060403)

Hotel Accommodation

Go To Japanese Page 日本語のページはこちら

1. Hotel TWINS MOMOCHI http://www.twinsmomochi.jp/
   - It takes about 5 minutes walk to the workshop site of WRTLT'06.
   - Convenient and economical.
   - LAN on the PC at Lobby but no internet connections in the room.
   - Japanese Web page only.
   - Reserve through the travel agency, Japan Travel Bureau (JTB).
2. JAL Resort Sea Hawk Hotel Fukuoka http://www.hawkstown.com/e_site/index.html
   - It takes about 10 minutes walk from the hotel to the workshop site of WRTLT'06.
   - Internet connections in most rooms.
   - Reserve through the travel agency, Japan Travel Bureau (JTB).
3. ARK Hotel Hakata http://hakata.ark-hotel.co.jp/
   - It takes about 10-15 minutes ride by bus (220 yen).
   - Internet connections in most rooms.
   - Japanese Web page only.
   - Reserve through the travel agency, Japan Travel Bureau (JTB).
4. HYATT Residential Suites Fukuoka http://www.hyatt-rsf.co.jp/english.html
   - It takes about 5 minutes walk from the hotel to the workshop site of WRTLT'06.
   - Can use internet connections in the room.
   - Reserve through the hotel Web Site, directly.
5. Many hotels are in Tenjin or Hakata area. But, a few have English Web sites.

   http://www.asiahotels.com/hl/Fukuoka-Japan.asp

   http://www.asiarooms.com/japan/fukuoka.html

   http://www.living-in-fukuoka.info/e/

Japan Travel Bureau (JTB) is the travel agency. You can make a reservation through it.

- ATS 2006 and WRTLT 2006 Hotel Reservation Guide (Word file).
- ATS 2006 and WRTLT 2006 Hotel Reservation Guide (PDF).
- Hotel Reservation Form (Word file).
- Hotel Reservation Form (PDF).

Please print out the form, fill out the form and send it to the travel agency by e-mail.

- Symposium Location Map.
- Hakata, Fukuoka Map.

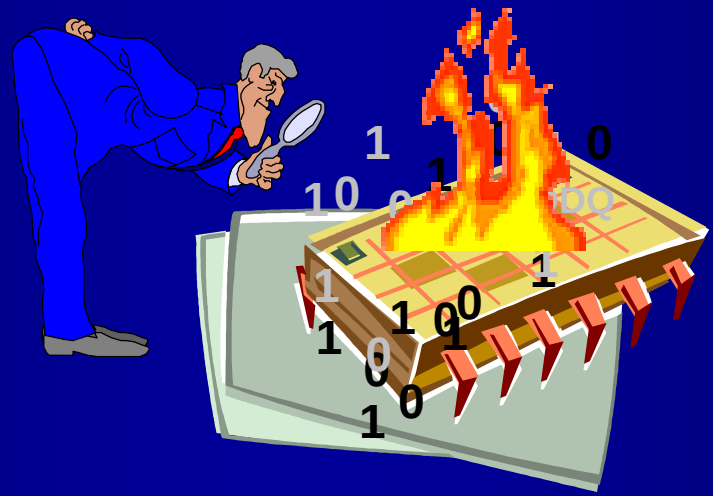
WRTLT '06

Fukuoka, JAPAN

Power Testing

P. Girard C. Landrault S. Pravossoudovitch A. Virazel

L.I.R.M.M. - CNRS / University of Montpellier - FRANCE



Outline

1. Introduction
2. Terminology and power modeling
3. Problems induced by test power
4. Techniques for low power testing
5. Summary and discussion

1. Introduction

ATE or Embedded Testing

Test Quality (with DFT)

- Fault Coverage
- Area Overhead
- Test Application Time
- Test Development Effort
- Test data volume

Test Power

Power consumed during test application

1. Introduction

Test power is higher than power in normal mode

It can be as high as twice the normal power [Zorian93]

Why ?

- the circuit is highly stressed and the switching activity is several times higher than in normal mode
- no definite correlation between consecutive test patterns
- the DFT circuitry is intensively used and low power functional devices are very often disabled during testing (scan for example)
- concurrent testing is often employed in SOC designs

1. Introduction

Test power is higher than power in normal mode

Consequences:

- increase of IC costs
- decrease reliability
- reduced autonomy (remote systems)
- performance certification

detailed description in part 3

2. Terminology and power modeling

Energy **= total switching activity generated during test**

- has impact on the battery lifetime during power up or periodic self-test of battery operated devices

Average Power **= Energy / test time**

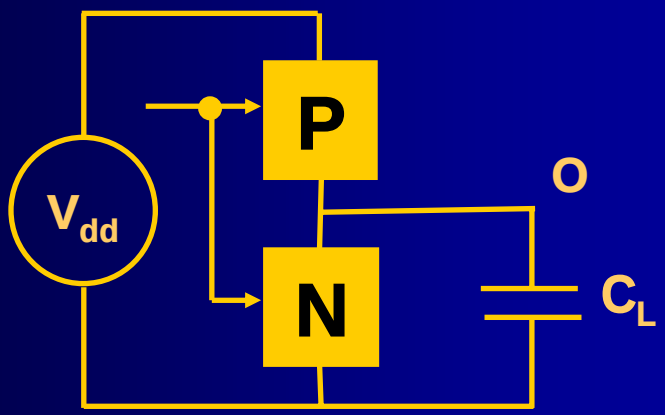
- has impact on the thermal load of the device and may cause structural damage to the silicon or reliability problems

Peak Power **= highest value of instantaneous power**

- determines the thermal and electrical limits of components and the system packaging requirements, may also cause structural damage to the silicon or reliability problems

2. Terminology and power modeling

Power consumed by a gate composed of 3 components



- Dynamic power: charge of output capacitance
- Short circuit power: Short circuit between power and ground during switching
- Leakage power

$$P_{dyn} = V_{dd}.I = V_{dd}.Q.1/T \text{ where } Q = C_L.V_{dd}$$

$$P_{dyn} = C_L.V_{dd}^2.N_{0\rightarrow1}.1/T$$
$$P_{dyn} = \frac{1}{2}.C_L.V_{dd}^2.N.1/T$$

2. Terminology and power modeling

Energy consumed after application of (V_{k-1},V_k)

$$E_{Vk} = \tfrac{1}{2} \cdot c_0 . V^2_{DD} \cdot \sum_i s(i,k) \cdot F_i$$

Total energy consumed during test application

$$E_{Total} = \tfrac{1}{2} \cdot c_0 . V^2_{DD} \cdot \sum_k \sum_i s(i,k) \cdot F_i$$

Average power consumed during the test session

$$P_{AVERAGE} = E_{Total} / (Length_{Test} \cdot T)$$

Peak power consumed during the test session

$$P_{PEAK} = \max_k P_{inst}(V_k) = \max_k (E_{Vk} / T)$$

2. Terminology and power modeling

Test Power Acting Parameters

Switching Activity 

- has impact on the energy, average power and peak power

Test Frequency

- has impact on the average power and peak power

Test Length

- has impact on the energy

2. Terminology and power modeling

Test Power Contributors

Combinational Toggling 

- switching activity in the combinational part of the circuit

Sequential Toggling

- switching activity in the flip-flops

Clock Toggling 

- switching activity in the clock tree feeding the circuit

3. Problems induced by test power

Thermal Effects

- heat produced during the functioning of a circuit is proportional to the dissipated power (Joule effect) and is responsible for die temperature increase
- too high temperature can provoke irreversible structural degradations (premature destruction)
- too high temperature may affect circuit performance or can have an impact on the ICs reliability (corrosion, electro-migration, hot-carrier-induced defects, dielectric breakdown, ...)

3. Problems induced by test power

Noise phenomena

- inductive phenomena due to current variation through inductive connections (probes for wafer testing, pins for packaged circuits)
- "ground bounce" or "V_{dd} bounce" may change the rise/fall times of some signals in the circuit causing some good dies to fail the test thus leading to yield loss
- IR drop (resistive effect) and crosstalk (capacitive effects) may lead to the same kind of problems particularly when at-speed transition testing is performed

3. Problems induced by test power

Product Costs

- expensive packages instead of plastic packages are needed for the removal of excessive heat
- cooling systems may be required

Autonomy

- for remote and portable systems powered by batteries where periodical self-tests are applied

Performance certification

- at-speed and delay testing under power limits becomes difficult

4. Techniques for low power testing

Techniques currently used in industry

Ad hoc solutions:

- over sizing power rails,
- over sizing or modifying packages and use of cooling systems
- test with reduced operation frequency (increase of test time and cost, dynamic faults masking)
- partitioning and appropriate test planning

However ...

proposed alternatives, solutions ...

4. Techniques for low power testing

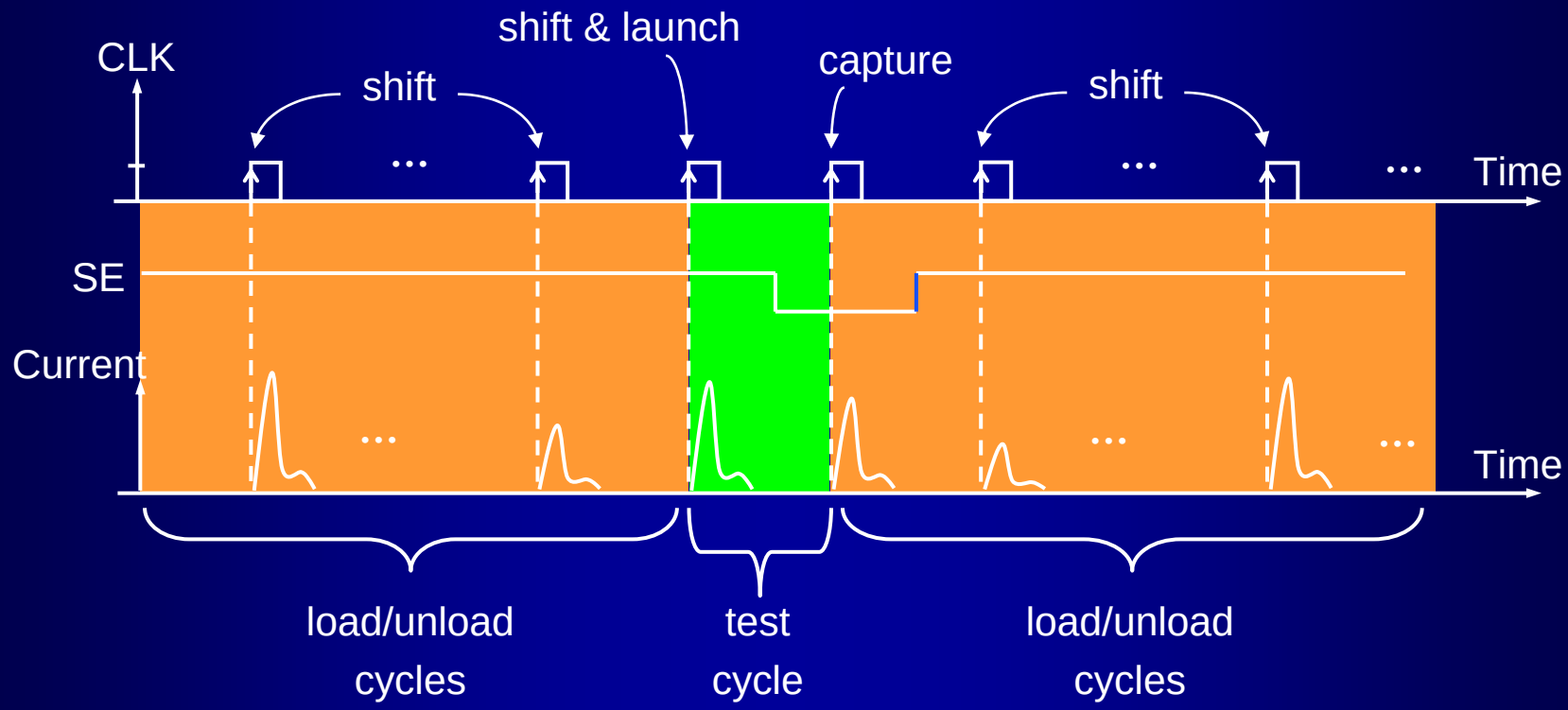
Low power scan Testing

Low Power BIST

Low Power techniques dedicated to special circuitry (compression, Rams)

4. Low power scan testing

Shift, Test Cycle and Capture Power



4. Low power scan testing

Use of Potential Test Pattern Flexibility (X's)

- the fraction of don't care bits (X's) in a given ATPG produced pattern is nearly always a very large fraction of the total available bits despite the application of state-of-the-art dynamic and static test pattern compaction techniques
- in classical ATPG, X's are randomly filled and then the resulting fully specified pattern is simulated to confirm detection of all targeted faults and to measure the amount of "fortuitous detection"

4. Low power scan testing

Use of Potential Test Pattern Flexibility (X's)

New ATPG with power aware objectives

- clever assignment of don't care bits in combinational (PODEM like) ATPG in order to minimize the number of transitions between two consecutive test vectors [Wang1994] [Wang1997]
- for sequential ATPG, optimization (by GA) under power constraints on a previously obtained redundant test set [Corno1998]
- minimizing the difference between the before-capture and after-capture output values of a scan flip-flop [Wen2006]

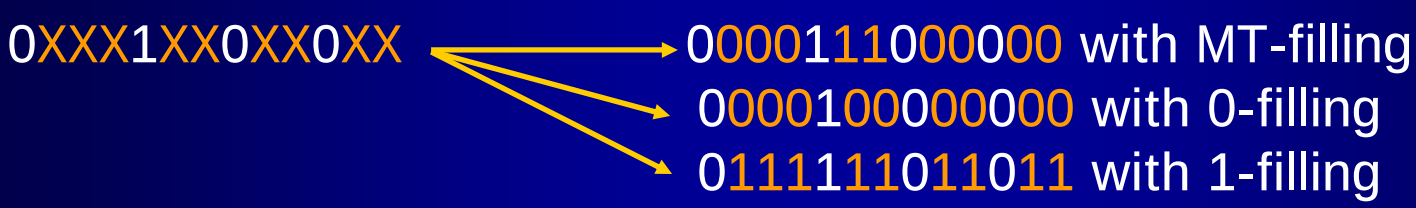
4. Low power scan testing

Use of Potential Test Pattern Flexibility (X's)

Use of Power aware X-filling techniques

• From a set of deterministic test cubes, the main goal of these techniques is to assign don't care bits of each test pattern so that the occurrence of transitions in the scan chain is minimized [Butler 2004] [Badereddine2006]:

- ❑ Adjacent filling or MT-filling
- ❑ 0-filling
- ❑ 1-filling



• Applicable at the end of the design process, no area overhead. Reduce test power consumption by reasonable increase of test length

4. Low power scan testing

Low power test vector compaction

- Static compaction minimizes the number of test cubes generated by an ATPG tool by merging test cubes that are compatible in all bit positions
- Conventional approaches target the minimum number of final test cubes
- [Sankaralingam 2000] used a greedy heuristic procedure for merging test cubes in a way that minimizes the number of transitions (use of weighted transition metric)
- Significant reductions in average and peak power consumption can be obtained by using this approach.

4. Low power scan testing

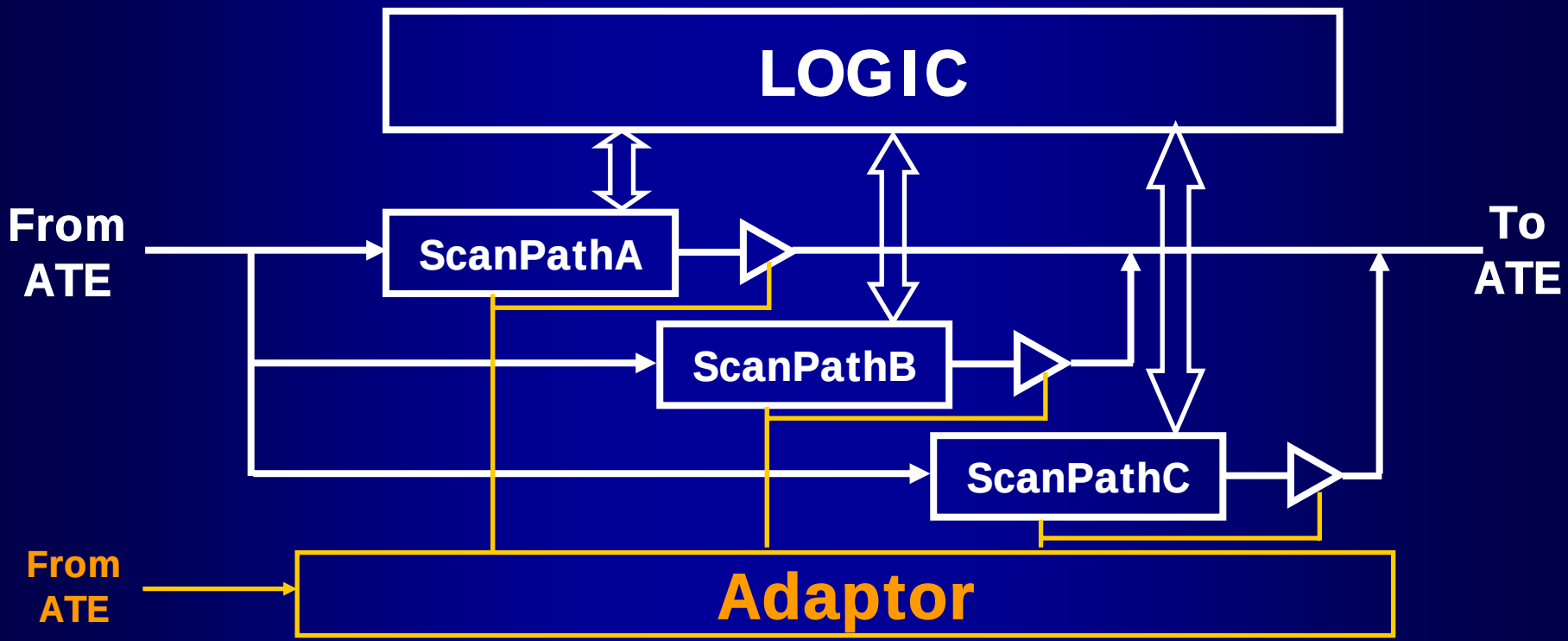
Scan Cell Ordering [Dabholkar98] [Girard02] [Higami02] [Kajihara02] [Sankaralingam02] [Sinanoglu02] [Girard03]

The switching activity is reduced by modifying the order in which the scan flip-flops are chained:

- the context is always ATE testing
- minimization of the number of transitions induced by scan-in and scan-out of the entire deterministic test set
- accounting for the routing constraints by using clustering techniques
- test length and fault coverage are unmodified
- average and peak power reduction are up to 66% depending on the routing constraints

4. Low power scan testing

Scan Architecture modification by insertion of new elements [Whetsel 2000 (SE), Saxena 2001 (Clk)]



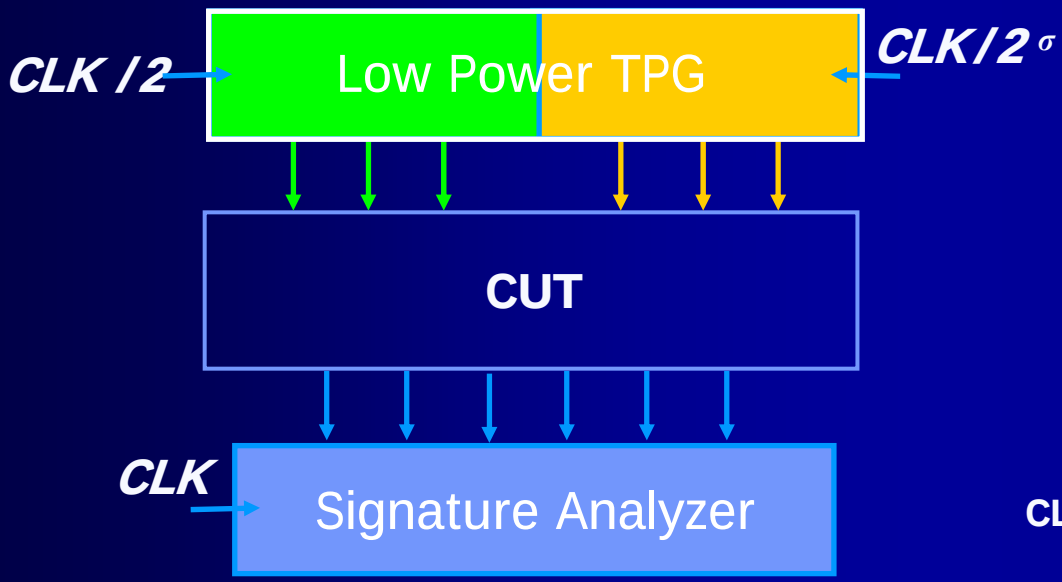
4. Low power scan testing

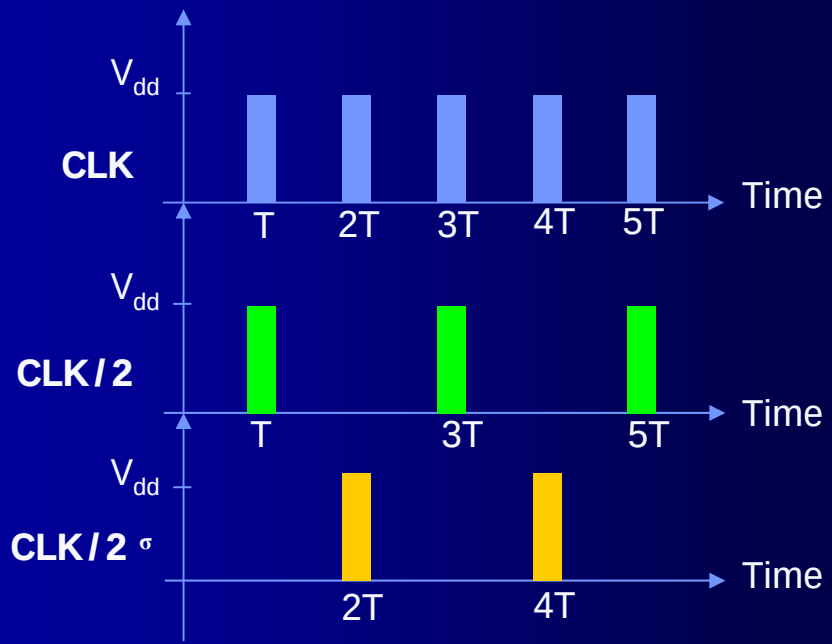
Scan Architecture modification by insertion of new elements [Lee 2000] [Sinanoglu2002] [Huang2001]

- use of buffers in multi-scan circuits to provoke a slight temporal shift between scan chains
- inserting logic elements (XOR gates) between scan FF in order to minimize the number of transitions occurring inside the scan chain
- multi-phase technique based on a token ring-like scan architecture

4. Low power scan testing

Scan Clock Splitting [Bonhomme2001]





4. Low power BIST

Basic BIST Reminders

- a ***test pattern generator*** (TPG) automatically generates test patterns for application to the inputs of the ***circuit under test*** (CUT)
- in-circuit TPGs constructed from LFSRs are most commonly used
- LFSRs are also used for ***output response analyzer*** (ORA)
- BIST is implemented as ***Test-per-scan*** (scan based BIST) and as ***test-per-clock***
- Test per scan is more often used even it is slower as its impact on the design flow is much more manageable and it is much cheaper

4. Low power BIST

Low Power BIST TPGs – [Wang97][Girard99][Wang99] [Zhang99] [Corno00] [Gizopoulos00]

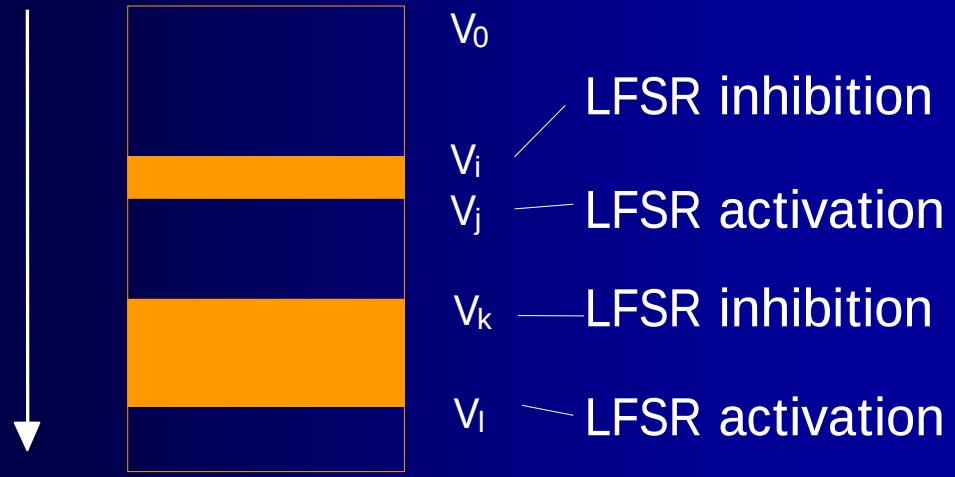
TPGs based on LFSRs (or Cellular Automata or Gray Counters) are carefully designed to reduce the activity at circuit inputs, thus reducing power consumption:

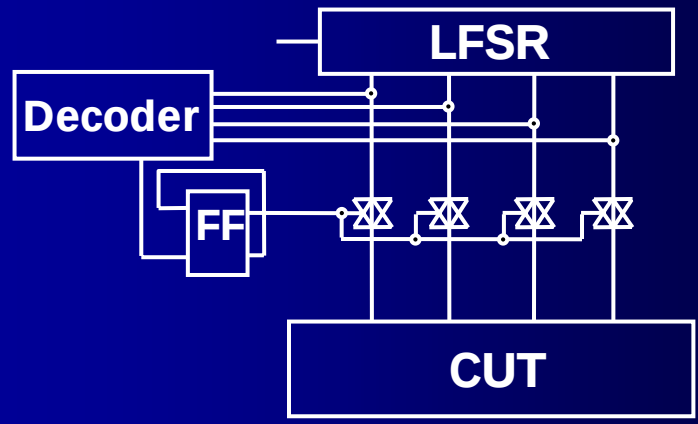
- by carefully choosing the seed of the LFSR (choice of polynomial has no real influence)
- by using two LFSRs running at different frequencies (use of the notion of transition density on inputs)
- by inserting translating logic between the LFSR and the CUT to obtain weighted random test vectors
- by using Gray counters producing consecutive test vectors with only one bit difference in the case of deterministic testing of data paths

4. Low power BIST

Vector Filtering Techniques – [Girard99][Wunderlich99] [Manich00]

Test Sequence



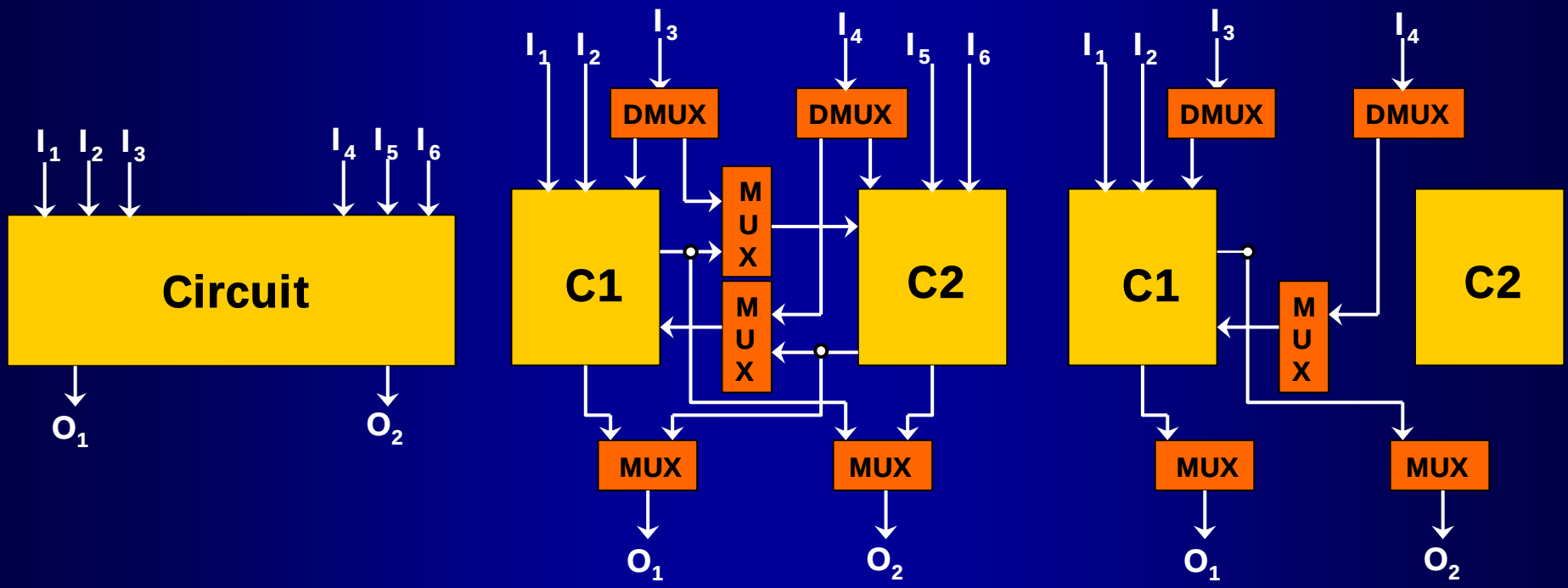


The goal is to prevent application of non-detecting (but power consuming) vectors to the CUT – minimizes average power without reducing fault coverage.

Proposed for LFSR-based test per clock or test per scan BIST methodologies

4. Low power BIST

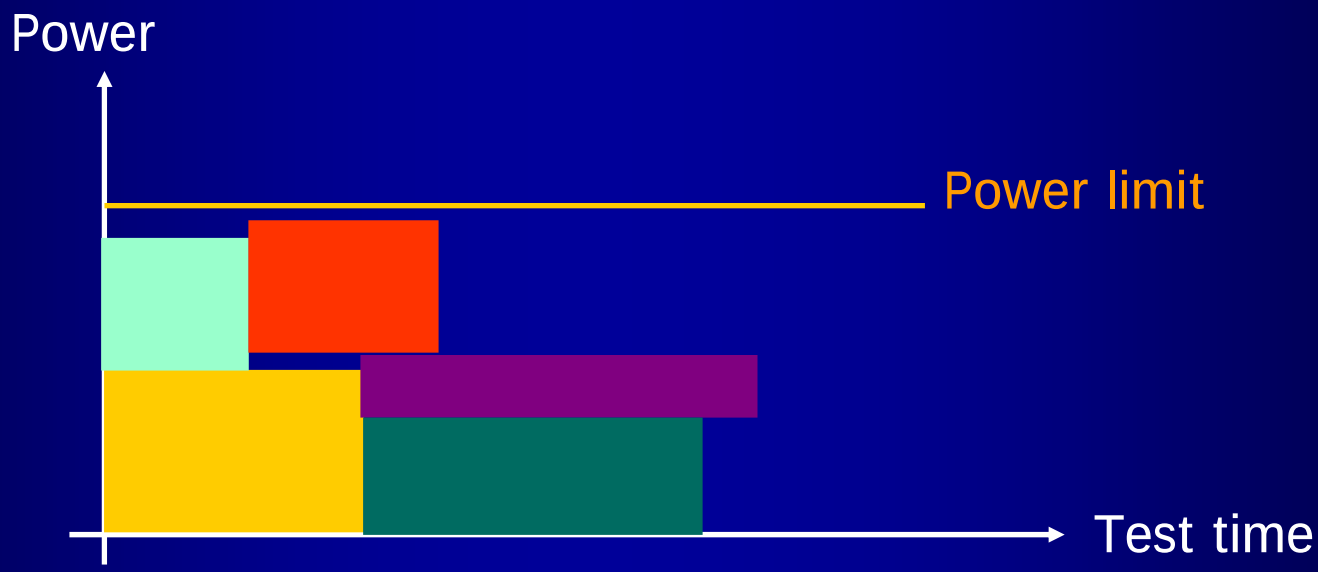
Circuit Partitioning Techniques for BIST – [Girard00]



It consists in partitioning the original circuit into structural sub-circuits so that each sub-circuit can be successively tested through different BIST sessions – FC and test time are unchanged without suffering a too large area increase

4. Techniques for low power testing

Test Scheduling Techniques – [Zorian93] [Chou94]



The goal of this well known scheduling techniques to determine the blocks of a complex design to be activated in parallel at each stage of the BIST test session in order to keep the power dissipation under the specified limits while optimizing test time (some of the blocks can share test resources)

4. Techniques for low power testing

Test Scheduling Techniques for SoCs – [Chou94] [Muresan00][Larsson01][Schuele01][Huang02][Iyengar02][Pouget03] [Ubar05]

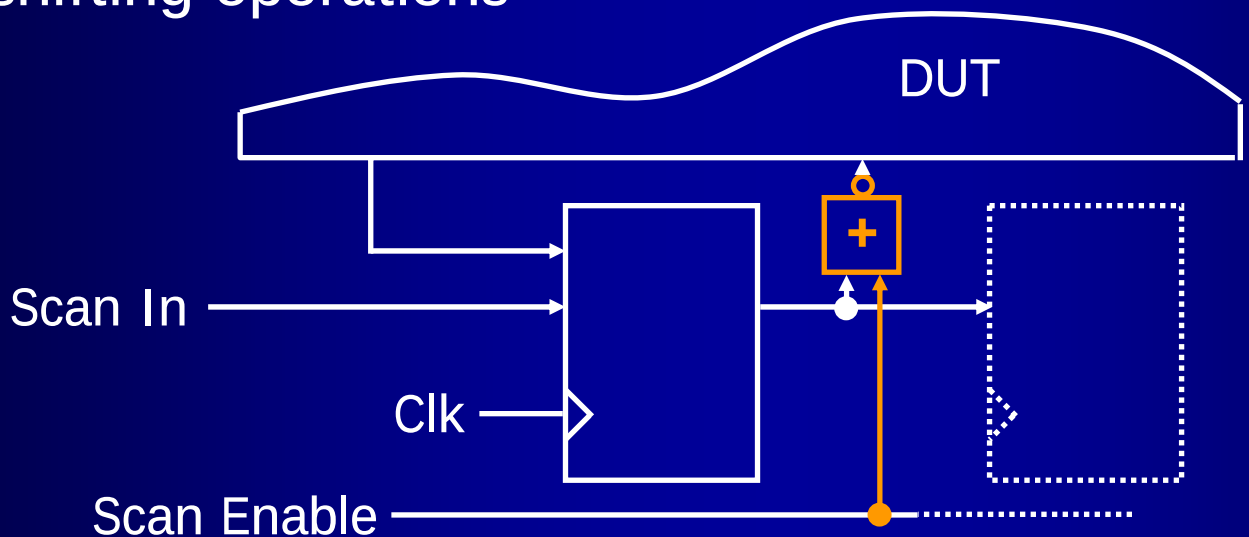
From a given power constraint, and considering a number of elements related to the test organization (fixed, variable, or undefined test sessions with or without precedence constraints) or to the test structure (test bus width, test resources sharing), these techniques allow to obtain the best solutions in terms of SOC test time.

Ubar minimizes the total test energy in an hybrid BIST test architecture

4. Low power scan testing

Shift Control Techniques

- [Huang1999] proposed to determine an input vector (on primary inputs), minimizing the switching activity in the combinational part during shifting operations
- [Hertwig1998] proposed to modify the scan FF to block transitions in the combinational part during shifting operations



4. Techniques for low power testing

Low Power Test Data Compression – [Chandra01] [Chandra02][Lee04][Badereddine06]

- Test data compression encodes a test set so as to reduce its size, enable to overcome the limited memory of the ATE and the bandwidth gap between ATE and CUT
- implies to have an on-chip decoder to decompress the data fed to the CUT
- use of 0-filling on test cubes and then encode with Golomb codes (run-length codes) for reducing the number of transitions
- improvement by using alternating run-length coding in place of Golomb coding
- for linear decompression, divide test cubes into blocks and code only the care ones, the others are generated by MT-filling

4. Techniques for low power testing

RAM low power testing: [Cheung96]

- The strategy is to modify a March test of the memory to reduce the number of transitions without decreasing the Fault Coverage and the memory overall test time.
- Write and read accesses and also the address counting scheme are rearranged.
- Each proposed test has the same fault coverage and time complexity as the original version,
- Reduction of power dissipation by a factor of two to sixteen
- Special design of the BIST circuitry is needed

4. Techniques for low power testing

RAM low power testing: [Dillilo06]

- pre-charge circuits have the role of pre-charging and equalizing the long and high capacitive bit lines
- pre-charge circuits are the principal contributor to power dissipation in SRAM (up to 70% of power dissipation)
- in functional mode the cells are selected in random sequence, and therefore all pre-charge circuits need to be always active while during the test mode the access sequence is known
- addressing sequence is fixed to “word line after word line” and the pre-charge activity is restricted only to two columns for each clock cycle: the selected column and the following one.
- 50% power savings with negligible area overhead

4. Techniques for low power testing

Reordering of test vectors: [Chakravarty94] [Dabholkar98] [Girard99]

- mainly targeting external testing without scan, or with enhanced scan (shadow scan register)
- original solution based on the search of Hamiltonian path in a graph representing the total transitions induced by vector pairs in the CUT (high CPU time),
- simplified solutions using either the Hamming distance between input test vectors or the induced activity function at each CUT's input
- power and energy savings of up to 50%

5. Summary and discussion

Lowering test power has been and is still now a focus of intense research and development.

Following points have been surveyed:

- test power parameters and contributors
- problems induced by an increased test power
- state-of-the-art techniques for low power testing

...

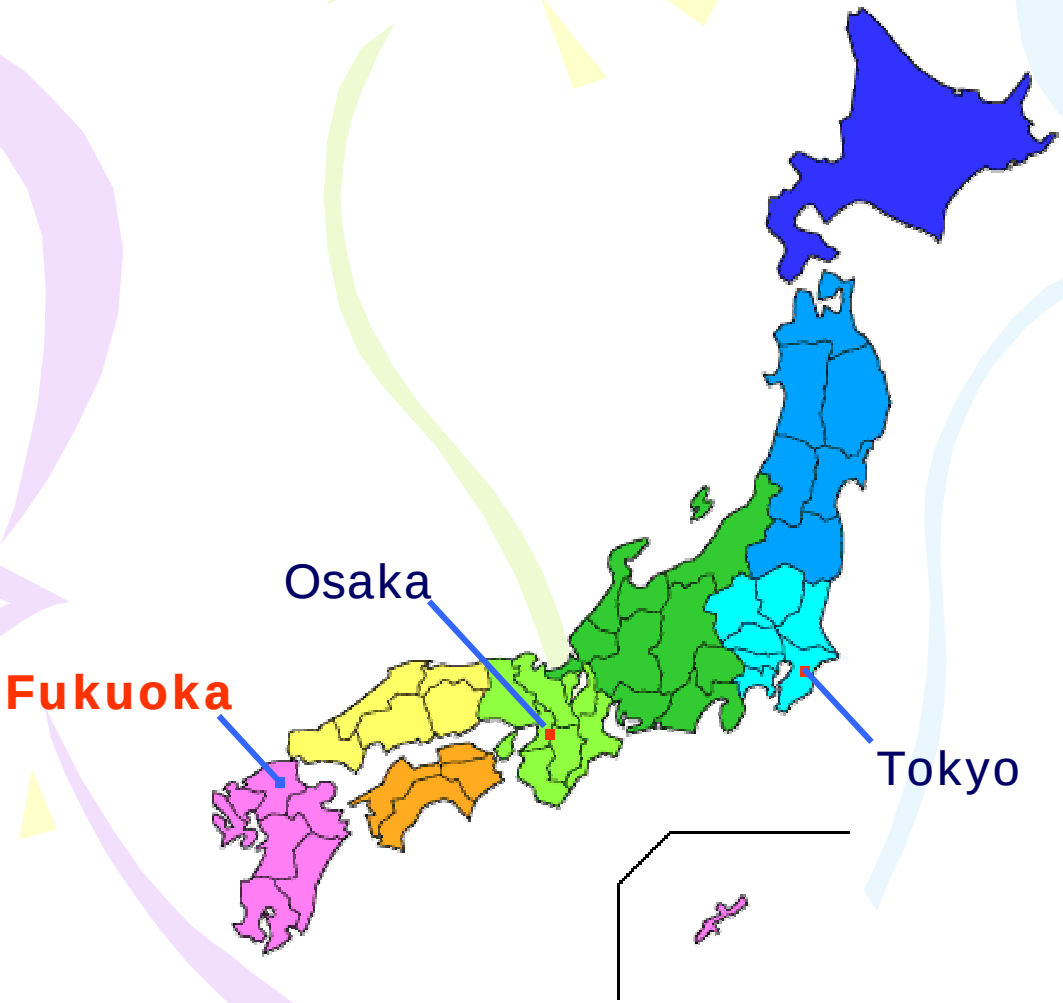
5. Summary and discussion

The selection of one of the reported techniques by a DfT engineer depends on:

- context (ATE testing, scan, BIST, ...)
- acting on the test sequence or the test architecture ...
- degree of freedom in relaxing some of the classical constraints ...
- impact on the circuit performance ...
- impact on the design flow ...
- ...

An introduction to the Host City

- Fukuoka -



Fukuoka
- The City -

- The biggest city on Kyushu Island
- Population: 1,380,790 as of April 1, 2004, and growing
- Average November temperature: 13°C
- Rich cultural heritages
- Energetic industrial and commercial activities
- Beautiful weather, great foods, and friendly people





Fukuoka
- Attractions -

Canal City Hakata
(Futuristic Shopping Center)

Tochoji Temple

Asian Art Museum

Fukuoka Tower

Kawabata
(Traditional Shopping Area)

Karashi Mentaiko
(Spicy Chilled Cod Roe)

Mizutaki
(Chicken-Vegetable Broth)

Ohori Park

Tonkotsu Ramen
(Hakata-Style Soup Noodle)

Hakata Doll

Nakasu
(Entertainment District)

Enjoyable City

福岡

Fukuoka
- Access -

◆ **By Air**

Served by Fukuoka Airport.

Easy connecting from major hub-airports in Japan.

① Narita International Airport (90 minutes)
② Haneda International Airport (90 minutes)
③ Kansai Int'l Airport (60 minutes)

Direct flights for many cities in Asia.

Beijing, Shanghai, Xi'an, Taipei, Hongkong, Seoul, Singapore, etc.

Domestic flights for all major cities in Japan.

◆ **By Rail**

Served by JR Hakata Station.

Fast Shinkansen service available.

① From Tokyo (5 hours 30 minutes)
② From Shin-Osaka (2 hours 30 minutes)

An introduction to the Workshop Site

Fukuoka System-LSI R&D Center

Fukuoka System-LSI R&D Center

- Access Map -

Fukuoka System-LSI R&D Center

- Access -

- **From Fukuoka Airport (45 Minutes)**

  Take Bus (Route#39)
  for Fukuoka Tower – South Entrance.

  Get off at Fukuoka Tower – South Entrance.

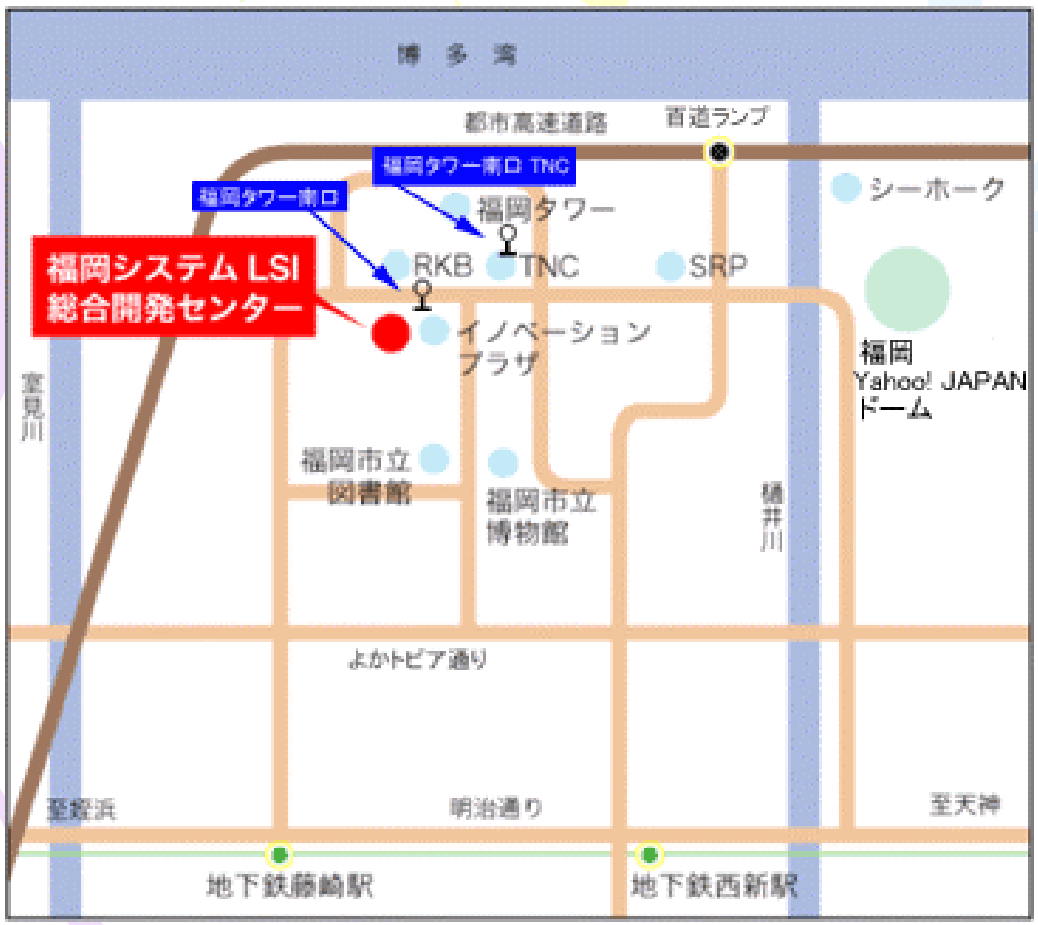
- **From JR Hakata Station (35 Minutes)**

  Take Bus (Route #39/#306/#312) at Bus Center Terminal 1F5
  for Fukuoka Tower – South Entrance.

  Get off at Fukuoka Tower – South Entrance.

Fukuoka System-LSI R&D Center

- Vicinity Map -



An introduction to Accommodation
- Hotels -

- **Fukuoka city is served by a large collection of hotels at fairly reasonable prices.**
- **Many hotels are in close distance (10~20 minutes by bus) from SRP.**
- **Two hotels are in walking distance (3~5 minutes by foot) from SRP.**
  - Sea Hawk Hotel
  - Hotel Twins Momochi
- **For more information on hotels in Fukuoka City:**
  http://www.asiahotels.com/hl/Fukuoka-Japan.asp

Sea Hawk Hotel

http://www.hawkstown.com/resortlife/index.html

High-quality resort hotel.
A 5-minute walk from SRP.
Possible reception site.

SEA HAWK
HOTEL & RESORT

Single: ￥13,125

Double: ￥22,050

Twin: ￥23,100

Hotel Twins Momochi

http://www.fcc-web.com/twm/

Convenient business hotel.
A 3-minute walk from SRP.

Single: ￥6,825
Double: ￥8,400
Twin: ￥10,500

WRTLT'06 ADVANCE REGISTRATION INSTRUCTIONS

Advance registration due: Oct. 13, 2006

For registration, **mail or fax** a registration form* (or a copy of the form) to:

Hideyuki Ichihara, WRTLT'06 Registration Chair
Faculty of Information Sciences, Hiroshima City University
3-4-1 Ozuka-higashi, Asaminami, Hiroshima, 731-3194 JAPAN
Fax: +81-82-830-1574 E-mail: ichihara@im.hiroshima-cu.ac.jp
Phone: +81-82-830-1569

No registration form will be accepted after **November 10, 2006** (postmarked cut-off). After Nov. 10, 2006, there will be on-site registration only.

Registration Fee:

Workshop registration fee includes admission to all technical sessions, coffee breaks, lunches, banquet and a copy of the workshop digest of papers. The student fee does not include banquet. The banquet ticket may be purchased separately by accompanying persons and students for 5,000 yen per person.

Before Oct. 13, 2006:

IEEE/CS Member*	Non-Member	Student Member / Life Member	Student
20,000 yen	25,000yen	7,500 yen	10,000 yen

* IEEE/CS member rate is also applied to IEICE member.

After Oct. 13, 2006:

IEEE/CS Member*	Non-Member	Student Member / Life Member	Student
25,000 yen	35,000 yen	9,000 yen	12,000 yen

* IEEE/CS member rate is also applied to IEICE member.

Payment:

Payment by bank transfer:

The account name must be written as:

WRTLT06 Masaki Hashizume Account No. 0301530
Shikoku bank (Bank # 0175)**, Ihoku branch** (Branch # 310)**, Japan**

For Japanese: 日本国内からの送金は銀行振込でお願いします。日本語では以下のようになります。
WRTLT06 ハシズメマサキ　四国銀行　渭北（イホク）支店　普通0301530

Payment by credit card:

Available for participants from abroad.

Refund Policy:

No refunds will be made unless written request for cancellation is received prior **Oct. 13, 2006**.

---

* The registration form is on the next page. It is also available from the WRTLT'06 web site:
http://www.ip.elec.mie-u.ac.jp/wrtlt06/

WRTLT'06, 7th Workshop on RTL and High Level Testing, Fukuoka, Japan, November 23-24, 2006

Registration Form

Please complete by typing or printing in block letters.

Title: ❑ Prof. ❑ Dr. ❑ Mr. ❑ Ms.
Last name:_____ First name:_____

Middle Name:_____
Affiliation / Company:_____
Mailing Address: ❑ Office ❑ Home
_____
_____
Phone: _____ Fax: _____

E-mail: _____
❑ IEEE/CS Member (No.:_____) ❑ IEICE Member (No.:_____)
Accompanying person, if any: _____

Registration Fee (Check one of the boxes):

Before Oct. 13, 2006:

IEEE/CS Member*	Non-Member	Student Member / Life Member	Student
❑ 20,000 yen	❑ 25,000 yen	❑ 7,500 yen	❑ 10,000 yen

* IEEE/CS member rate is also applied to IEICE member.

After Oct. 13, 2006:

IEEE/CS Member*	Non-Member	Student Member / Life Member	Student
❑ 25,000 yen	❑ 35,000 yen	❑ 9,000 yen	❑ 12,000 yen

* IEEE/CS member rate is also applied to IEICE member.

Payment (Check one of the boxes):

❑ Payment by bank transfer**:** I will remit/have remitted the fee on_____(date) under the name of_____(name of remitter) to the account of:

WRTLT06 Masaki Hashizume Account No. 0301530
Shikoku bank (Bank # 0175)**, Ihoku branch** (Branch # 310)**, Japan**

For Japanese: 日本国内からの送金は銀行振込でお願いします。日本語では以下のようになります。
WRTLT06 ハシズメマサキ　四国銀行　渭北（イホク）支店　普通0301530

❑ Payment by credit card: (for participants from abroad)

❑Visa ❑MasterCard

Card No.: _____ Expiration Date: _____/_____

Card Holder (printed): _____

Date: ____/____/_____

Advance Registration Deadline: October 13, 2006
For advance registration, **mail or fax** this form (or a copy of this form) to:

Hideyuki Ichihara, WRTLT'06 Registration Chair
Faculty of Information Sciences, Hiroshima City University
3-4-1 Ozuka-higashi, Asaminami, Hiroshima, 731-3194 JAPAN
Fax: +81-82-830-1574 E-mail: ichihara@im.hiroshima-cu.ac.jp
Phone: +81-82-830-1569

No registration form will be accepted after **November 10, 2006** (postmarked cut-off). After November 10, 2006, there will be on-site registration only.

宿泊施設

1. ホテルツインズももち http://www.twinsmomochi.jp/
    - WRTLT'06の会場に一番近いホテル（徒歩５分程度）
    - ホテルはビジネスホテルで、きれい.
    - １階にはローソンあり.
    - インターネット接続は有線・無線ともない．ロビーにはインターネット接続のPCが置いてある.
    - Japan Travel Bureau (JTB)で予約可能.部屋数が限られていますお早めに予約を.
2. JALリゾートシーホークホテル福岡 http://www.hawkstown.com/hotel/
    - WRTLT'06の会場まで歩いて１０分程度.
    - 部屋内でインターネット接続可能（リニューアル後の客室のみ）
    - Japan Travel Bureau (JTB)で予約可能．部屋数が限られていますお早めに予約を.
3. ARK http://hakata.ark-hotel.co.jp/honkan/index.html
    - 博多の中心である天神に位置するホテル
    - 会場近くのバス停まで福岡年高速経由のバスで１０分～１５分 (220 円).
    - インターネットは客室で利用可能
    - Japan Travel Bureau (JTB)で予約可能. .部屋数が限られていますお早めに予約を.
4. ハイアット レジデンシャルスイート福岡 http://www.hyatt-rsf.co.jp/
    - WRTLT'06の会場まで歩いて５分程度.
    - 持参PCを部屋のインターネットコネクションに接続可能
    - JTBでは予約を承っておりませんので、ホテルのWebから直接予約してください.
    - 家族用の滞在型ホテルですので，複数で部屋をシェアするのも手.
5. Many hotels are in Tenjin or Hakata area. But, almost all the hotels don't have English Web sites.

    http://www.asiahotels.com/hl/Fukuoka-Japan.asp

    http://www.asiarooms.com/japan/fukuoka.html

http://www.living-in-fukuoka.info/e/

6. 博多駅周辺，天神周辺にも多数のホテルがあります。日本からの参加者はバスに乗るのも不自由しないと思いますので，博多駅周辺、天神周辺もわりと便利です。インターネット接続ができて５０００円後半から７０００円くらいまでのホテルが多数あります。
7. 公共の宿

   ウェル大濠荘 http://www.kjp.or.jp/hp_113/ 大濠公園の近く。WRTLT'06会場までは歩くと２０分強かかるが、黒門-->福岡タワー方面バスも出ている.（時刻表）
8. 上記１－３までのホテルは、JTBで下記のフォームを使って予約できます。とくに１のホテルは便利ですが、ホテル直接のWebサイトからですともう部屋の残りは少ないという情報が参加者より寄せられています。WRTLTではJTBに依頼して「ツインズももち」をある程度おさえてありますが、部屋数に限りがありますのでお早めに。

- ATS 2006 and WRTLT 2006 Hotel Reservation Guide (Word file).
- ATS 2006 and WRTLT 2006 Hotel Reservation Guide (PDF).
- Hotel Reservation Form (Word file).
- Hotel Reservation Form (PDF).

上記の申込書を利用して電子メールでJTBに申し込みください。部屋数に限りがあります。

- ATSとWRTLTの開催場所（百道浜）の地図はこちら
- 博多地区の地図はこちら
- 西鉄バスのWebはこちら